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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,816	08/21/2002	Hou-Yuan Lin	GIGP0001USA	7780

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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EXAMINER	
MOORE, PAOLO DAVIDIAN	
ART UNIT	**PAPER NUMBER**
2187	4

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,816	LIN, HOU-YUAN	
	Examiner	Art Unit	
	Paolo Davidian Moore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☒ Claim(s) *4-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10004816 has a total of 7 claims pending in the application. There is 1 independent claim and 6 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 CFR '1.63**.

Claim Objections

3. Claims 4-7 are objected to because of the following informalities: inconsistent terminology. In line 1 of each claim, **"managing"** should read as **"management"**.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7 rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Klein (Pat. No. 6349051 B1).

6. As per claim 1, the admitted prior art in Fig. 1 discloses a BIOS for storing an access control program and outputting a control signal when the access control program is activated; an integrated chipset that receives the control signal from BIOS access control program; and a DRAM memory module socket comprising three access control mode input ports.

7. The prior art in Fig. 1, however, fails to teach that the integrated chipset has a pair of general purpose input/output (GPIO) terminals for outputting a first and second control output; and a pair of switches for respectively receiving the first access control signal and the second access control signal and selectively outputting the first access control signal and the second access control signal to the three access control mode input ports respectively according to the first control output and the second control output.

8. Klein in Fig. 4 teaches the use of a bus switch, controlled by a control input, as to connect its input data bus to one of its output data buses. This bus switch is situated between a memory controller, which supplies the control input, and a memory module.

9. It would be obvious to a person of ordinary skill in the art at the time the invention was made to insert a switching device having a reasonable number of switches (e.g. one or two) in the data path of the access control mode input ports of the memory

module socket of the admitted prior art in order to reduce the parasitic capacitance of the data bus and increase the speed of data transfer (Klein col. 2 lines 52-54). It follows that this modification would necessitate control signals for the switching device. It is common practice in the art to use the GPIO terminals of many commercially available integrated chipsets to provide these control signals.

10. As per claim 2, the admitted prior art in Fig. 1 discloses an integrated chipset that receives the control signal from BIOS access control program.

11. As per claim 3, the admitted prior art in Fig. 1 discloses a pair of access control mode output ports that are an Error Correction Code (ECC)/Clock Enable (CKE) mode output port and a Data Input Output Mask (DQM)/CKE mode output port.

12. As per claim 4, the admitted prior art in Fig. 1 fails to teach a DRAM module socket that is a DDRDRAM socket.

13. As it is common practice in the art, it would be obvious to a person of ordinary skill in the art at the time the invention was made to use a commercially available DDRDRAM socket for high data rate memory applications.

14. As per claim 5, the admitted prior art in Fig. 1 fails to teach a DRAM module socket that is a RDRAM socket.

15. As it is common practice in the art, it would be obvious to a person of ordinary skill in the art at the time the invention was made to use a commercially available RDRAM socket for high data rate memory applications.

16. As per claim 6, the admitted prior art in Fig. 1 discloses that three access control mode input ports are an EEC mode input port, a CKE mode input port and a DQM mode input port.

17. As per claim 7, the admitted prior art in Fig. 1 fails to teach the use of switches that respectively receive the first control output and the second control output to selectively output the first access control signal and the second access control signal to two of the three access control mode input ports.

18. This further claimed limitation of selective output to "two of the three access control mode input ports" would follow necessarily when the admitted prior art device is modified in the manner mentioned in the rejection of claim 1. It was been known and commonly practiced in the pertinent art to use a switching device to selectively couple data buses in a combinatorial manner.

Relevant Art Cited by the Examiner

19. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

20. The following references teach the use of **programmable switching circuitry** used to interface with **memory modules**:

U.S. Patent Number	**Figure(s)**
5,781,717	1
5,878,240	1
6,070,217	1
6,518,972 B1	5, 6
6,662,260 B1	2-6, 9

21. The following reference teaches the use of **BIOS** to control the **Suspend To RAM** functionality of the **memory modules**:

U.S. Patent Number	**Figure(s)**
6,542,996 B1	1

22. The following references teach the use of the **BIOS** to control the **EEC** functionality of the **memory modules**:

U.S. Patent Number	**Figure(s)**

5,978,952	1
6,212,631 B1	1

23. The following reference teaches the use of the **GPIO terminals** of a **chipset** to control a **switch matrix** for USB ports:

U.S. Patent Number	**Figure(s)**
6,256,700	1

Conclusion

24. Per the instant office action, claims 1-7 have received a first action on the merits and are subject of a first action non-final.

Direction of Future Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paolo Davidian Moore whose telephone number is 703-305-4667. The examiner can normally be reached on M-F 8:00AM-5:00PM.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PDM

HIEP T. NGUYEN
PRIMARY EXAMINER